

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau(43) International Publication Date
30 January 2003 (30.01.2003)

PCT

(10) International Publication Number
WO 03/009361 A2

(51) International Patent Classification⁷: H01L 21/288, 21/768

(21) International Application Number: PCT/US02/23429

(22) International Filing Date: 22 July 2002 (22.07.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/306,758 20 July 2001 (20.07.2001) US
60/384,643 31 May 2002 (31.05.2002) US

(71) Applicant: NUTOOL, INC. [US/US]; 1645 McCandless Drive, Milpitas, CA 95035 (US).

(72) Inventors: BASOL, Bulent, M.; 3001 Maple Avenue, Manhattan Beach, CA 90266 (US). TALIEH, Homayoun; 2211 Bentley Ridge Drive, San Jose, CA 95138 (US). UZOH, Cyprian, E.; 625 Parvin Drive, Milpitas, CA 95035 (US).

(74) Agents: JAKOPIN, David, A. et al.; Pillsbury Winthrop LLP, 1600 Tysons Boulevard, McLean, VA 22012 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

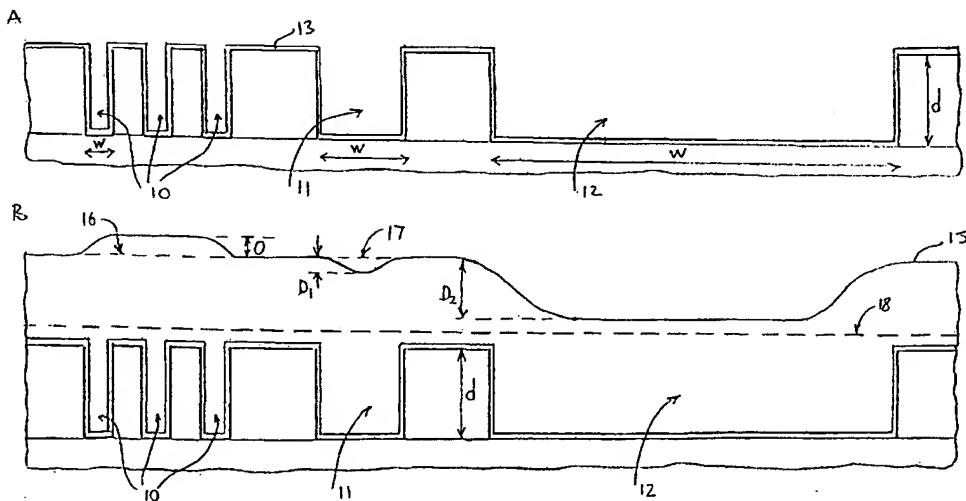
(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PLANAR METAL ELECTROPROCESSING



WO 03/009361 A2

(57) Abstract: The present invention relates to a method for forming a planar conductive surface on a wafer. In one aspect, the present invention uses a no-contact process with electrochemical deposition, followed by a contact process with electrochemical mechanical deposition. In another aspect the no-contact process with electrochemical deposition uses a solution tailored to this no-contact process, and the contact process with electrochemical mechanical deposition uses a different solution tailored to this contact process.

PLANAR METAL ELECTROPROCESSING

5 1. FIELD OF THE INVENTION

[0001] The present invention relates to manufacture of semiconductor integrated circuits and, more particularly to a method for planar deposition and polishing of conductive layers.

10 2. DESCRIPTION OF THE RELATED ART

[0002] Conventional semiconductor devices generally include a semiconductor substrate, such as a silicon substrate, and a plurality of sequentially formed dielectric interlayers such as silicon dioxide and conductive paths or interconnects made of conductive materials. Copper and copper-alloys have recently received considerable attention as interconnect materials because of their superior electro-migration and low resistivity characteristics. The interconnects are usually formed by filling copper in features or cavities etched into the dielectric layers by a metallization process. The preferred method of copper metallization is electroplating. In an integrated circuit, multiple levels of interconnect networks laterally extend with respect to the substrate surface. Interconnects formed in sequential layers can be electrically connected using vias or contacts.

[0003] In a typical process, first an insulating layer is formed on the semiconductor substrate. Patterning and etching processes are performed to form features or cavities such as trenches and vias in the insulating layer. Then, a barrier/glue layer and a seed layer are deposited over the patterned surface and a conductor such as copper is electroplated to fill all the features. However, the plating process, in addition to filling the features with copper, also deposits excess copper over the top surface of the substrate. This excess copper is called an "overburden" and needs to be removed during a subsequent process step. In standard plating processes this overburden copper has a large topography since the Electrochemical Deposition (ECD) process coats large features on the wafer in a conformal manner. For example, a wafer with 0.5 micron deep features may be coated with 0.8 micron thick copper by the standard ECD process, to assure complete, defect-free filling of all the features, including those that are wider than about 5 microns. The resulting copper surface then may have a topography that has a step of about 0.5 microns over the large features. Conventionally, after the copper plating, CMP process is employed to first globally planarize this topographic surface and then to reduce the thickness of the overburden copper layer down to the level of the surface of the barrier layer, which is also

later removed leaving conductors only in the cavities. CMP is a costly and time consuming process. High pressures used in the CMP processes also damage low-k dielectrics, which are mechanically weaker than the silicon oxide. Therefore, minimizing CMP step in an integration process is a goal for all IC manufacturers. The topography on the wafers also causes problems for the CMP process. Specifically, the large steps such as the 0.5 micron step of the above example over the large features such as 100 micron wide trenches or bond-pads, cause dishing defects after CMP. Therefore, both in terms of cost and enabling features, it is very attractive to have processes that have the ability to yield thinner copper deposits with reduced surface topography on wafers.

[0004] During the copper electrodeposition process, specially formulated plating solutions or electrolytes are used. These electrolytes typically contain water, acid (such as sulfuric acid), ionic species of copper, chloride ions and certain additives which affect the properties and the plating behavior of the deposited material. Typical electroplating baths contain at least two of the three types of commercially available additives such as accelerators, suppressors and levelers. It should be noted that these additives are sometimes called different names. For example, the accelerator may be referred to as a brightener and the suppressor as a carrier in the literature. Functions of these additives in the electrolyte and the role of the chloride ion are widely known in the field (see for example, Z. W. Sun and G. Dixit, "Optimized bath control for void-free copper deposition", Solid State Technology, November 2001, page. 97), although the details of the mechanisms involved may not be fully understood or agreed upon.

[0005] Electrodeposition process needs to fill all the features, small and large, on the substrate. Figure 1A schematically shows the cross sectional view of an exemplary wafer surface with high-aspect ratio vias 10, a medium aspect-ratio trench 11, and a small aspect-ratio pad 12, coated with a barrier/seed layer 13, which is shown as one layer to simplify the drawing. As is well known in the field, aspect ratio is the ratio of the depth, d , of the features to their smaller lateral dimension or width, w . In our example the depth, d may range from 0.1 microns to 2.0 microns, although deeper features may also be used for certain applications such as packaging applications. The width of the vias 10 may be sub-micron in size and their aspect ratio (d/w) may be in the range of 1-10. The trench 11 may have an aspect ratio of 0.1-1 and the pad 12 may have an aspect ratio of less than 0.1. For a feature depth of for example 0.5 microns, the vias may be 0.1 micron wide, the trench 11 may be 2 micron wide and the pad may be 20 microns wide.

[0006] Figure 1B shows the substrate of Figure 1A after copper deposition carried out by prior art methods. The solid line 15 indicates the typical topography of the copper film resulting from a typical ECD process employing an additive package containing two additives,

accelerator and suppressor species. It is well known that these additives help bottom-up filling of the high aspect-ratio vias 10 with copper. The mechanism of bottom-up fill, however, becomes less and less effective as the aspect ratio of the features become smaller and smaller, and the deposition becomes more and more conformal. The result is shown in Figure 1B as a small step

5 D1 over the medium size feature or trench 11 and a large step D2 over the large feature or pad 12. It should be noted that magnitude of these steps over the various size features is at most as large as the feature depth, d. The over-fill, O, shown over the dense array of vias 10 is typically observed in copper films deposited by the electrolytes containing two-component additive package of this example. As can be seen in Figure 1B, the surface topography of the copper film 10 is large and this presents challenges in the CMP step as described earlier.

[0007] Several developments have been provided by prior art methods to improve the copper topography depicted by the solid line 15 in Figure 1B. To reduce or eliminate the over-fill O, a third additive, leveler, is added into the electrolyte formulation. By controlling the concentration of the additive carefully, the profile of copper over the dense array of vias 10 could 15 be made flat, which is shown as the dotted line 16 in Figure 1B. U.S. Patent 6,346,479 B1 describes a method where copper is deposited in a non-conformal electroplating process to fill a portion of the features. A second electroplating process is then performed to conformally deposit copper in the remaining unfilled portion of the openings or features. Such an approach may yield a flat profile over dense array of small features such as vias 10 of our example, as well as 20 possibly over the medium size features such as trench 11 of our example as depicted by dotted lines 16 and 17, respectively. However, as disclosed in U.S. Patent 6,346,479 B1 the second electroplating process conformally deposits copper over the substrate, and therefore can not eliminate the large step D2 over the large features such as the pad 12 shown in our example of Figure 1B. U.S. Patent 6,350,364 B1 describes a method of electroplating copper in trenches 25 where a first copper deposition step has a first ratio of brightener-to-leveler concentration and a second copper deposition step has a second ratio of brightener-to-leveler concentration that is less than the first ratio of brightener-to-leveler concentration. This way it is reported that the step D1 of Figure 1B can be reduced. As is well known in the field copper electroplating additives are not operative in the very large features with very small aspect-ratios such as the pad 12 of 30 Figure 1B. Therefore, the step D2 is not expected to be much reduced or eliminated by such approaches. D2 only gets reduced and eliminated if a very thick copper layer with thickness value close to half the width of the largest feature on the wafer is plated (see e.g. U.S. Patent 5,256,565, October 26, 1993). However, this is not practical considering the fact that many interconnect designs involve feature sizes well above 10 microns.

[0008] As the above review demonstrates, some of the prior art techniques aiming to obtain relatively flat copper topography on patterned wafer surfaces may be applicable for the class of wafers with large or medium aspect-ratio features. However, many IC interconnect designs contain features with a wide variety of aspect ratios on a given wafer surface. Especially 5 in multi-level interconnect structures the width of the high-current-carrying lines increase while their aspect-ratios decrease at the higher wiring levels. Therefore, an approach that has the capability of reducing or eliminating surface topography of copper over features with a large range of aspect ratios is needed.

[0009] A technique that can reduce or totally eliminate copper surface topography for 10 all feature sizes is the Electrochemical Mechanical Processing (ECMPR). This technique has the ability to eliminate steps D1, D2 and overfill O shown in the example of Figure 1B, and provide thin layers of planar conductive material on the workpiece surface, or even provide a workpiece surface with no or little excess conductive material. This way, CMP process can be minimized or even eliminated. The term "Electrochemical Mechanical Processing (ECMPR)" is used to 15 include both Electrochemical Mechanical Deposition (ECMD) processes as well as Electrochemical Mechanical Etching (ECME), which is also called Electrochemical Mechanical Polishing (ECMP). It should be noted that in general both ECMD and ECME processes are referred to as electrochemical mechanical processing (ECMPR) since both involve 20 electrochemical processes and mechanical action on the workpiece surface. An exemplary flat copper surface profile resulting from an ECMPR is shown as the flat dotted line, 18, in Figure 1B.

[00010] Descriptions of various ECMPR approaches and apparatus, can be found in the following patents, published applications and pending applications, all commonly owned by the assignee of the present invention: U.S. Patent No. 6,126,992 entitled "Method and Apparatus for 25 Electrochemical Mechanical Deposition," U. S. Application No. 09/740,701 entitled "Plating Method and Apparatus that Creates a Differential Between Additive Disposed on a Top Surface and a Cavity Surface of a Workpiece Using an External Influence," filed on December 18, 2001 and published as US Patent Application on February 21, 2002 with patent application No. 20020020628, U.S. Application filed on September 20, 2001 with serial number 09/961,193 30 entitled "Plating Method and Apparatus for Controlling Deposition on Predetermined Portions of a Workpiece", U.S. Application with serial number 09/960,236 filed on September 20, 2001, entitled "Mask Plate Design.," and U.S. Application No. 10/155,828 filed on May 23, 2002, entitled "Low Force Electrochemical Mechanical Processing Method and Apparatus." These methods can deposit metals in and over cavity sections on a workpiece in a planar manner.

3. SUMMARY OF THE INVENTION

[00011] The present invention relates to a process for forming a near-planar or planar layer of a conducting material, such as copper, on a surface of a workpiece using an ECMPR technique.

5 [00012] In one aspect, the present invention includes positioning the front surface of the workpiece in close proximity to a workpiece surface influencing device. Thereafter, the plating solution containing the conductive material is flowed to the front surface of the workpiece through the channel in the workpiece surface influencing device. An electric potential is applied between the workpiece and the electrode both of which are in physical contact with the plating 10 solution, thereby allowing a conductive material to be formed on the front surface of the workpiece using an electrochemical deposition process. In a subsequent electrochemical mechanical deposition process, the front surface of the workpiece is then swept or polished using a top surface of the workpiece surface influencing device as an electric potential and the plating solution is applied. In the next step, an electric potential having a polarity opposite the electric 15 potential used in the electrochemical deposition process and the electrochemical mechanical deposition process is applied to the workpiece and the electrode.

[00013] In another aspect, the process preferably uses at least two separate plating solution chemistries to form a near-planar or planar copper layer on a semiconductor substrate that has features or cavities on its surface.

20 [00014] At a first stage, a plating process that is optimized for the defect-free filling of the small features is carried out. During this stage, plating is done in a non-touch mode with no mechanical sweeping on the wafer surface and uses a first plating solution with first additive chemistry that is optimized for the best gap-fill performance. This chemistry may contain accelerators and suppressors and optionally levelers.

25 [00015] The second stage uses an ECMPR touch-process, typically including at least an ECMD process, with a second plating solution that has a second additive chemistry, which is optimized specifically for this planar deposition or planarization step. This second chemistry, for example, may contain only one or two of the three additives that may be used for the first stage.

30 4. BRIEF DESCRIPTION OF THE DRAWINGS

[00016] The above and other features and advantages of the invention are further described in the detailed description which follows, with reference to the drawings by way of non-limiting exemplary embodiments of the invention, wherein like reference numerals represent similar parts of the invention throughout several views and wherein:

[00017] Figures 1A illustrates a cross sectional view of an exemplary wafer that requires application of a conductor thereover;

[00018] Figure 1B illustrates a cross sectional view of the exemplary wafer of Figure 1A that has had a conductor applied thereover using conventional methods;

5 [00019] Figure 2 illustrates a cross sectional view of the exemplary wafer of Figure 1A that has had a conductor applied thereover using methods according to the present invention;

[00020] Figure 3 illustrates a portion of an exemplary ECMPR system that can be used to practice the present invention;

10 [00021] Figure 4 shows a first structure that is formed on the front surface of the workpiece;

[00022] Figure 5 illustrates a first layer deposited into the cavities and on the top surfaces of the workpiece;

[00023] Figures 6A, 6B and 7 illustrate various profiles that can be achieved;

[00024] Figures 8A and 8B illustrate formation of defects;

15 [00025] Figure 9 illustrates further planarizing the growing deposition layer;

[00026] Figures 10 illustrates a profile when a no-contact electroetching process is used;

20 [00027] Figure 11 illustrates a profile when a contact electroetching process is further used;

[00028] Figure 12 illustrates a dual damascene structure getting filled with a conductor;

[00029] Figures 13A-13C illustrate profiles of an exemplary wafer at different stages of the process according to the present invention;

25 [00030] Figures 14A and 14B illustrate focused ion beam images of a wafer processed in various manners according to the present invention;

[00031] Figure 15 illustrates a system of modules that can be used to implement the process according to the present invention; and

[00032] Figure 16 illustrates a process supply system for use with a single process module.

30 5. DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[00033] The process of the present invention relates to a process for forming a near-planar or planar layer of a conducting material, such as copper, on a surface of a workpiece using an ECMPR technique such as ECMD. The process of the present invention preferably uses at least two separate plating solution chemistries to form a near-planar or planar copper layer on a 35 semiconductor substrate that has features or cavities on its surface. The unique feature of the

present invention is the fact that it can be applied to substrates with features or cavities of a wide variety shapes and dimensions. For example the substrate may have high-aspect ratio small size features, such as sub-micron size vias or trenches, as well as very low aspect-ratio features such as larger than 10 micron wide trenches and larger than 20 micron size pads or channels. There

5 may even be larger than 500 micron features on this exemplary wafer. At a first stage of the present invention, a plating process that is optimized for the defect-free filling of the small features is carried out. During this stage, plating is done in non-touch mode with no mechanical sweeping on the wafer surface. The no-touch process uses a first plating solution with first additive chemistry that is optimized for the best gap-fill performance. This chemistry may

10 contain accelerators and suppressors and optionally levelers. At this stage the small and mid size features are entirely filled with copper while the larger size features are partially or completely conformally coated with a copper layer. An example of a copper layer profile resulting from the first stage of the present invention is shown in Figure 2 as profile 30. It should be noted that all the small features are filled with copper, there is a small step over the medium size feature and a

15 large step over the large feature. This first stage of the present invention may be continued until the copper level over the largest feature becomes substantially the same as the level of the top surface of the insulating layer. In this case the smaller step may be reduced but the step over the large features stays substantially the same.

[00034] A second stage of the present invention uses an ECMPR touch-process, typically including at least an ECMD process, with a second plating solution that has a second additive chemistry, which is optimized specifically for this planar deposition or planarization step. This second chemistry, for example, may contain only one or two of the three additives that may be used for the first stage. Depending upon the duration of the touch-step a copper profile that is substantially flat (shown as profile 31) or absolutely flat (shown as profile 32) can be obtained. As the duration of the touch-step is increased the surface becomes flatter and flatter. In any case the reduced, flatter topographies of profiles 31 and 32 in Figure 2 as compared the prior-art large topographies of Figure 1B, increase the efficiency of the CMP process and reduce CMP related defects such as dishing and erosion.

[00035] Figure 3 shows an exemplary ECMPR system 100 that can be used to practice the present invention. The ECMPR system includes a workpiece-surface-influencing device (WSID) 102 such as a mask, pad or a sweeper, a carrier head 104 holding a workpiece 106 such as a wafer, and an electrode 108. The wafer can be a silicon wafer to be plated with copper using the ECMD process. The WSID 102 is used during at least a portion of the ECMD when there is physical contact and relative motion between a front surface 110 of the wafer 106 and the top surface 112 of the WSID 102. During ECMD, the top surface 112 of the WSID sweeps the

surface 110 of the wafer 106 while an electrical potential is established between the electrode 108 and the surface of the wafer. Alternately, in some cases potential is established right after WSID surface 112 sweeps the surface 110 of the wafer. In other words establishment of the potential and sweeping of the substrate surface by the WSID do not have to be simultaneous or 5 continuous as described in detail in previous applications cited above. Channels 114 of the WSID allow a process solution 116 such as a copper plating electrolyte to flow to the surface of the wafer 106.

[00036] As described above, one aspect of the present invention is the usage of a no-contact process using electrochemical deposition, followed by a contact process using 10 electrochemical mechanical deposition. This process sequence can be implemented using the same solution in both the contact and the no contact processes, or different solutions. Accordingly, a separate description will be provided for each. It should be understood, however, that certain aspects of the process sequence as described using the same solution can be used for the process sequence using different solutions, and vice versa.

15 [00037] Same Solution Process Sequence

[00038] When using the same solution for the entire process sequence, an exemplary copper plating solution may be a copper base solution such as a solution containing CuSO₄, H₂SO₄, Cl⁻ and additives. The additives are generally chemicals called suppressors, accelerators, levelers and brighteners etc., which affect the grain size, morphology, and filling of the small 20 features as well as smoothness of the deposited copper. Such additives are well known in the copper plating industry. The copper plating solution used in this invention may also comprise alternative additive chemistries. One such alternative additive chemistry is disclosed in the pending U.S. Application No. 09/544,558 entitled "Modified Plating Solution for Plating and Planarization and Process Utilizing Same" which is commonly owned by the assignee of the 25 present invention. Other alternative chemistries, agents can also be used with the plating solution of the present invention to affect the properties of the deposited material and are within the scope of this embodiment of the invention.

[00039] The preferred process implementing this embodiment will now be described. Figure 4 shows a first structure 400 which is formed on the front surface 110 of the workpiece 30 106 as shown in Figure 3. The first structure 400 is comprised of a patterned layer 402, preferably an insulating layer such as silicon oxide, formed on a base layer. The first structure 400 may be formed using well known patterning and etching techniques pursuant to metal interconnect design rules. In this embodiment, the insulating layer 402 includes cavities or gaps, namely a first cavity 404, a second cavity 406 and a third cavity 408, separated from one another 35 by interlayer regions 410. Each cavity 404, 406, 408 is defined by a bottom wall 412 and side

walls 414. The thickness of the inter layer regions 410 is determined as the distance between the bottom wall 412, or the base layer 110 top surface and the top surface 416 of the interlayer regions 410. In this example, the thickness of the interlayer regions 410 is equal to the depth of the cavities 404, 406 and 408. The top surfaces 416 of the interlayer regions 410 are also called

5 field regions.

[00040] In this embodiment, the cavities 404, 406, 408 can be formed such that the first cavity 404 may be a via or a narrow trench, the second cavity 406 may be a mid-size trench or a large via, and the third cavity 408 may be a trench or a large pad. In this respect, the first cavity 404 may have a width of less than 1 micrometers. The second cavity 406 may have a width of 1-10 5 micrometers, and the third cavity 408 may have a width of more than 5 micrometers. The depth of the cavities may be larger than 0.3 to 10 micrometers, but preferably 0.3-5 micrometers. At this point of the process, although not shown in the drawings, typically one or more thin layers of barrier or glue layer materials, for example, Ta, TaN, Ti, TiN, or WN can be deposited, using well known processes in the art, as a barrier or glue layer. Multiple layers of different 15 barrier materials, such as bilayers formed with sequential deposition of Ta and TaN or Ti and TiN can also be constructed. Subsequently, a thin film of copper is deposited as the seed layer on top of the barrier layer for the subsequent electroplated copper layer. The copper seed layer provides a base layer on which nucleation and growth of the subsequent deposition layer can occur.

20 [00041] Referring to Figure 5, a first layer 418 is deposited into the cavities 404, 406, 408 and on the top surfaces 416. The deposition process is performed using the exemplary system 100 described above. It is known in the art that copper electroplating solutions are formulated with additives that promote bottom up plating in narrow features/cavities. When workpiece with various size features are coated with copper using these electrolytes, the small 25 features, i.e., typically features that are smaller than 1 micrometer, are filled up easily and quickly with copper plating from the bottom of the cavity towards its top. Large features are coated in a conformal manner because additives can diffuse in and out of such features without impediment. Medium size features behave somewhat in between the two extremes.

[00042] In operation, initially, the front surface 110 shown in Figure 3 is plated without 30 making contact with the mask plate 102, (i.e., the workpiece 106 is held in close proximity of the mask plate 102 and moved during the plating). During this stage of the process, the gap between the wafer front surface and the surface of the mask plate is preferably about 1-4 millimeters (mm). This process step will be referred to as "no-contact" plating hereinafter. Referring back to Figure 5, at this stage of the process, the depositing material, which forms the first layer 418, fills 35 the first cavity 404 completely through bottom-up filling process and covers the walls and the

bottom of the third cavity 408 in a conformal fashion. Further, during the process, the material deposited into the second cavity 406 partially fills it in a somewhat bottom-up fashion. At this stage of the process, although a portion of the first layer 418 partially fills the second cavity 406 and makes it smaller, the remaining opening still maintains its high aspect ratio (depth D / width W), (i.e., D>W). It is understood that the second cavity 406 may be any cavity that is partially filled and that can be used to determine if the D>W condition exists. The no-contact plating may be continued as long as D>W condition exists in any of the cavities. Preferably, contact plating may not be initiated as long as the D>W condition exists. As will be described below, if the contact plating is initiated with D>W condition existing, defects may form.

[00043] Accordingly, as shown in Figures 6A and 7, depending on the process parameters used, no contact plating may result in a second layer 420 having two types of surface profile, namely flat profile (Figure 6A) and overfill profile (Figure 7) respectively. In the preferred flat profile, as shown in Figure 6A, as the no-contact plating process is continued and the second layer 420 is coated on the first layer 418, the aspect ratio of the second cavity 406 is smaller such that the width W of the cavity becomes larger than the depth D. That is, W>D condition exists. This condition may also be expressed in terms of the thickness of the selected regions of the deposited layer and the corresponding growth rate for that selected thickness value. As shown in Figure 6B, if r_b is the growth rate from the bottom wall of the second cavity 406 and r_w is the growth rate from the top of the side walls of the second cavity 406, the above given condition W>D can also be expressed approximately as $W_0 - 2 r_w t > (D_0 - r_b t)$, where W_0 and D_0 are the initial width and the depth of the cavity before the deposition, and t is the deposition time. It should be noted that the barrier and seed layers are not shown in any of the figures for the purpose of clarification.

[00044] Referring to the case of overfill profile (Figure 7), as the no-contact plating fills the first cavity 404 an overfill feature 421 such as a bump may form above the first cavity 404. During the copper plating process, such bumps are possible and formed due to the overfilling of the cavities. Although mechanism is not fully understood, it is believed that such bumps form due to preferential or accelerated adsorption of growth accelerating additive species in the small cavities. In such morphologies, due to the existence of the bump 421, in the subsequent contact plating stage, as opposed to the case of the flat profile, a thick deposition layer is required to fill the cavities 406, 408 and to cover the bump 421. This is time consuming and reduces system efficiency. Therefore, the flat profile is the preferred surface profile in this embodiment. However, if the bumps are formed, the second step of the process eliminates them by planarizing the surface.

[00045] Referring back to Figure 6A, flatness of the second layer 420 may be obtained using various techniques such as using flatness enhancing agents in the electrolyte solution or using a pulse power supply to energize the anode and the cathode. Flatness enhancing agents may be exemplified as levelers. Levelers are well known chemicals in the electroplating technology and used to effectively suppress the growth of bumps on the depositing layers. A pulse power supply or a variable voltage power supply can also minimize or eliminate the over fill bump. A technique called reverse pulse plating process may be used to obtain flat surface profiles over small features. In this approach, the voltage pulses make the workpiece surface periodically cathodic to deposit copper on it and anodic for a shorter time to etchback a portion of the deposited material so that flatness of the layer can be achieved. The pulse power supply can also be used during the second step or the contact plating and third step or the electroetching step of the process of the present invention. Referring back to Figures 6A and 6B, once the $W_0 - r_w t > (D_0 - r_b t)$ condition is satisfied for all the remaining features (i.e., the mid-size and the large features), the process is continued with the "contact" plating stage of the process, or a second stage of the process, to completely fill the cavities. At the "contact" plating stage of the process, the front surface 110 is contacted to the top surface of the mask plate 102, while the deposition process continues. If the contact plating is initiated without satisfying the $W > D$ condition, defects may form.

[00046] Figures 8A and 8B exemplifies formation of such defects. As shown in Figure 8A, when the contact plating is initiated the mask plate 102 sweeps or mechanically influences the top portion 418A of the layer 418 but not an inner portion 418B and a mouth portion 418C covering the second cavity 406 side walls and the bottom wall. This in turn reduces the growth rate at the top portion 418A in comparison to both the inner portion 418B and the mouth portion 418C. Further the mechanical influence increases lateral growth rate of the copper at the mouth portion 418C in comparison to the inner portion 418B since it creates an additive differential between the inner portion 418B. This situation can be seen in Figure 8B where as consecutive layers 419A, 419B, 419C are coated with contact plating, the layers 419A-419C grow faster at locations covering the mouth portion 418C than the inner portion 418B. Portions of the layers 419A-419C covering the top portion 418A grow slowly due to the mechanical influence created by the contacting mask plate. Such non conformal growth pattern eventually forms a defect 423, often a hole, entrapping electrolyte solution which is an unwanted situation in electroplating.

[00047] As shown in Figure 9, the mechanical influence created by the contacting mask plate 102 further planarizes the growing deposition layer, and if the overfill profile is used, the mechanical influence removes the bump 421 as well (see Figure 7). This results in a third deposition layer 424, which is a substantially planarized layer, on the workpiece 106. The

contact step of the process may proceed in such manner that the workpiece 106 may make contact with the mask plate 102 intermediately (i.e., in a discontinuous fashion). This still results in planarized layer and smoothes the top layer. Further, such contact and no-contact action may be repeated multiple times.

5 [00048] In the following stage of the process, by reversing the polarization of the electrodes (i.e., by applying negative potential to anode electrode and by applying positive potential to the workpiece), the layer 424 can be electroetched down to a predetermined thickness over the interlayer regions. In this third step, electroetching process may be performed using the same electrolyte solution used during the electrodeposition stage and using the same system
10 above. As in the case of electrodeposition, the electroetching may be also carried out by "no-contact" electroetching and "contact" electroetching process steps. Accordingly, as illustrated in Figure 10, with the no-contact electroetching process, thickness 'd' of the layer 424 can be reduced down to thickness A in a planar manner. As illustrated in Figure 11, with the application
15 of the contact electroetching process, contacting mask plate 102 reduces the thickness of the layer 424 in a planar fashion, down to thickness B.

20 [00049] Contact and no-contact electroetching can be used sequentially and multiple times using the same or different process parameters such as by employing different current levels, different wafer pressure levels and different rotational and lateral velocities. If contact and no-contact electroetching processes are performed in a multiple fashion, the process may be terminated with contact electroetching process. As mentioned above, the contact step smoothes the layer. The thickness B may be less than the depth D_0 of the cavities 404, 406 and 408, and preferably less than half of the depth ($D_0/2$) of the cavities. The third step of the process may be performed in the same electrolyte or solution that is used for the deposition process. Further, this step may be performed in the same process module that the deposition is carried out and
25 subsequent to the deposition process.

20 [00050] The method of the above embodiment can fill cavities of any shape and form. One example, a dual damascene structure 500, is shown in Figure 12. The dual damascene structure 500 has a via 502 and a trench 504 formed in an insulator 506. The via 502 may be a narrow via, and the trench 504 may be a mid size or a larger trench. If the above process is used, in first step of the process or no contact step, the depositing material fills the via 502 and
30 conformally coats the trench 504 with a first layer 508. In a second step, or contact step, of the process, the depositing material fills the trench completely with a second layer 510 and the mechanical influence created by the contacting mask plate 102 planarizes the growing second layer 510. In the third step, a layer 512 that is formed by sequentially depositing layers 508 and
35 510 is electroetched down to a predetermined thickness 'C' as shown in Figure 12.

[00051] Different Solution Process Sequence

[00052] The embodiment that uses different solutions for the no-contact process with electrochemical deposition and the contact process with electrochemical mechanical deposition will now be described.

5 [00053] Figure 13A shows the front surface 110 of the wafer 106 as it is electroplated using a first electroplating solution 120. The surface 110 may include small features 122, a mid size feature 124 and a large feature 126. The small size features may have a width less than a micron while the mid size features may have 1 to 5 micron width range. Large features may have a width larger than 10 microns. The features 122, 124, 126 are formed in an insulating 10 layer 128 that is formed on the semiconductor wafer 106. A barrier layer 130 such as Ta, TaN or their composite Ta/TaN coats the inside of the features and the top surface 132 of the insulating layer 128. The top surface 132 is also called the "field region". A seed layer (not shown) such as a thin copper layer is coated on the barrier layer. During the process, the wafer 106 is placed 15 away from the WSID (no-touch plating) and the first electroplating solution is flowed through the WSID to wet the front surface 110 of the wafer 106 while the wafer is rotated and moved laterally. Once an electrical potential applied between the wafer and the electrode, i.e., anode, (shown in Figure 2), a first copper layer 134a is formed. The first copper layer 134a fills the small and mid size features in bottom-up fashion but conformally coats the large feature because 20 of its large width.

20 [00054] In the first stage of the process, the WSID acts as a shaping plate. It is important that the channels of the WSID not only allows the process solution to flow to the surface of the wafer, but also shapes the plating current density and thus the resulting thickness profile of the deposited copper layer. The distribution, shape and size of the openings may introduce regions of low, intermediate, and high deposition rates above the WSID. By moving 25 the wafer over these regions during the process a desired thickness profile, e.g., a uniform thickness profile, of the depositing layer is obtained. An exemplary process of thickness profile control is disclosed in U.S. Patent Application No. 09/760,757 filed on January 17, 2001 entitled "Method and Apparatus for Electrodeposition of Uniform Film on Substrate," which is commonly owned by the assignee of the present invention. If desired, this plating step can be 30 carried out without the WSID if other means are provided to yield a uniform deposit.

35 [00055] In this embodiment, the first electroplating solution 120 may comprise at least two additives to enhance bottom up filling of the small features without any voids, seams and other defects. For example a high-acid plating electrolyte containing 0.8-2 ml/l of Cubath® ViaForm™ Accelerator available from Enthone-OMI®, West Haven, CT and 6-12 ml/l of Cubath® ViaForm™ Suppressor marketed by the same company may be used in the basic

plating bath chemistry which contains sulfuric acid, copper sulfate, water and chloride ions. Low acid versions of the plating chemistry may require quite different concentrations of accelerators and suppressors (such as an accelerator concentration of about 4-8 ml/l, and suppressor concentration of 2-4 ml/l for the case of Enthone low acid chemistry). During the process, the accelerators allow bottom up growth of copper in the small features that are filled quickly. The suppressor molecules which are adsorbed at the top of the openings of the small features slow down the copper growth therein, thus avoiding both premature closing of these passages and formation of voids. In addition to the accelerator and suppressor species, levelers may also be added in the formulation to reduce or eliminate the over-fill phenomenon discussed before in this application. Levelers get adsorbed preferentially on high-current density regions of the plated surface and help reduce this current density and thus protrusions that would have resulted. A leveler concentration of 0.5-2 ml/l may be used for this purpose in addition to the accelerator and suppressor species in the exemplary high acid chemistry mentioned above. An exemplary leveler which is sold under the brand name Cubath® ViaForm™ Leveler is available from Enthone-OMI®.

[00056] As illustrated in Figure 13B, once the no-touch plating with the first plating solution is completed, an ECMD touch-plating stage using a second plating solution 136 forms a second layer 134b that coats the first copper layer in a non-conformal fashion, depositing more materials into the cavities and less onto the surface regions where WSID sweeps. During this touch-plating process, as the second plating solution 136 is delivered onto the first copper layer 134a, WSID touches and mechanically sweeps the part of the first layer 134a that is located on the field regions and over the small and mid size features. Combined with the chemistry of the second plating solution, the sweeping action of the WSID slows down the growth of the copper layer on the field region and above the small features which are already filled and accelerates growth of the copper layer in the large features, thus planarizes the overall Copper deposit. It should be noted that the touch-plating stage of the process may be terminated before total planarization is achieved if the degree of planarization achieved at that point is adequate for simplifying the overburden removal process such as a CMP process, which follows the deposition process. In this embodiment, the additive chemistry of the second plating solution is optimized for the touch-plating step. For example, the second plating solution 132 may not contain any levelers. Furthermore, the accelerator-to-suppressor ratio in the second electrolyte may be higher than the ratio in the first electrolyte. Referring back to the exemplary high acid electrolyte mentioned above the accelerator concentration in the second electrolyte may be in the range of 2-10 ml/l, whereas the suppressor concentration may be in the 2-8 ml/l. This can be done because all the small features have already been filled on the wafer by the first plating step

and therefore there is no danger of causing void formation in such features by these new additive concentrations, which if used during the first stage process would result in non-optimal filling of the small features. The second electrolyte may even contain a single additive which is an accelerator. The present inventors observed that although single additive baths containing only 5 suppressors or only accelerators could be used for planarization in an ECMD process, planarization was more efficient for the baths containing just accelerators compared to baths containing just suppressors.

[00057] Figure 14A shows the Focused Ion Beam (FIB) image of a 5-micron wide trench on a wafer which was coated with copper using an ECMD apparatus and a copper sulfate electrolyte comprising Enthone Via-Form high acid VMS solution and 8ml/l of Cubath® ViaForm™ Leveler. A charge of 4 A-min was passed between the 200 mm diameter substrate and a copper anode during this process and a WSID was in contact with the wafer which was rotated at 50 rpm. As can be seen from the image in Figure 14A there is relatively more copper deposited into the feature than onto the top surface of the substrate indicating partial 10 planarization. Figure 14B shows the FIB cross-section taken from the same location of a similar wafer, which was processed similarly, however this time in another copper sulfate electrolyte comprising Enthone Via-Form high acid VMS solution and 2.2 ml/l of Cubath® ViaForm™ Accelerator. It is clear that copper deposition rate into the feature is higher in this case than the 15 case in Figure 5a indicating better planarization efficiency. The copper film in the 5-micron trench of Figure 14b is completely planar. This example illustrates that the solution chemistry 20 may be optimized for best planarization of a substrate during the touch-plating stage of the present invention.

[00058] The present invention allows optimization of the chemistry for the first stage of the process separate from the optimization of the chemistry for stage 2. This is important 25 because although it is possible to use the same chemistry for both the first and second stage of the ECMPR as described in the above mentioned patents and patent applications, it is attractive and beneficial to have the ability to optimize chemistry for the two stages independent from each other as will be further described below.

[00059] Concentrations and types of additives used in the first stage of the subject 30 process may vary depending upon the nature of the additives, nature of the small features, nature of the barrier/seed layers, etc. For example, some accelerator species containing sulfur react with weak seed layers. If the seed layer is very thin on the side-walls of the vias for a specific wafer, it may be necessary to reduce the accelerator-to-suppressor ratio in the electrolyte in the first stage of the process that is employed to coat this specific wafer. For other wafers with other 35 types of seed layers it may be necessary to further adjust the relative concentrations of additives

to obtain the best gap fill performance. If the over-fill over the dense array of small features presents a problem, it may be necessary to include leveler into the formulation in addition to the accelerator and suppressors.

[00060] The electrolyte chemistry, which is adjusted for best gap fill in the first stage 5 may not be the best for the second stage of the process when planarization takes place. For example, levelers are known to get attracted to high current density regions on the wafer surface. However, ECMD process is known to accelerate growth in cavities on the substrate surface by increasing the deposition current density in such cavities compared to the top surface of the wafer swept by the WSID. Therefore, levelers in an electrolyte used for the second stage of the process 10 may lower the planarization efficiency. This is an example of how presence of an additive (such as a leveler) in the process electrolyte may be favored during the first stage (no-touch step) of the process, whereas its presence may not be necessary or desired during the second stage (touch plating step). Similarly, a higher accelerator-to-suppressor ratio may be desirable in the second stage than for the first stage of the process as described before. The experiment of Figure 14B 15 indicated that an electrolyte containing only accelerator species may be successfully used in the second stage of the process, although such a formulation may not be successfully used for the first stage. Use of only one additive for the second process step may reduce the total additive consumption, simplify additive measurement and control systems, reduce costs and improve planarization efficiency increasing throughput. Total impurity content of the deposited film may 20 also be reduced by this approach.

[00061] In accordance with the principles of the present invention the first and the second stages of the process may be either performed in the same process module or multiple process modules. If the same process module approach is used to perform both stages, the first 25 and second stages are performed sequentially, and using a first solution for the first stage and a second solution for the second stage. As fully described above, the first solution chemistry includes additives enhancing bottom up filling of the features on the wafer. And, the second solution chemistry includes only one or two of the three additives that may be used for the first stage and is optimized specifically to obtain a planar copper layer. If there are multiple process modules, the first stage may be carried out in a first or first group of process modules with the 30 first solution chemistry, and the second stage may be carried out with a second or second group of process modules using the second solution chemistry. Following the two-stage deposition, the wafer is cleaned and planar or near-planar copper overburden is removed using the CMP or other (e.g., electropolishing) removal methods. The copper overburden may be removed before or after an annealing step.

[00062] It should be noted that after the second stage of the present process, optionally a third and even a fourth step can be used to reduce the thickness of the copper overburden. After the second stage of the process, the copper removal process may be performed as a third stage of the process that employs either an electrochemical etching or polishing stage or an ECME (electrochemical mechanical etching) stage. The removal process may be also performed using both steps sequentially as a third and fourth stage, for example, a no-touch etching step that is followed by a touch ECME, or a touch ECME followed by a no-touch etching. Thin planar deposits can be obtained by first depositing a planar layer using the ECMD technique at the first and second stages, and then electroetching this planar film in the same electrolyte or an electroetching solution by reversing the applied voltage. This way the thickness of the deposit may also be reduced in a planar manner. In fact, etching may be continued until all the metal on the field regions is removed. These techniques may be performed subsequent to second stage and using the second solution as an electroetching solution while reversing the polarity of the applied voltage and rendering the workpiece surface more anodic compared to the electrode.

10 Alternatively, a third solution comprising an electroetching solution may replace the second solution at the third stage and a fourth stage of the process, for example a no-touch electroetching (third stage) followed by a touch ECME (fourth stage). In this respect, a fourth stage such as a touch ECME process stage may be performed using a fourth solution.

15

[00063] Figure 15 exemplifies a system 150 using multiple modules A, B, C and D. In this exemplary configuration, the modules A and B may be ECD or ECMD modules to perform the first stage of the process with a first process solution. The second stage of the process may be performed in module C, which may also be an ECMD module, using the second process solution. Module D may be an ECME module to perform the above described third stage, such as a no-touch stage electroetching or ECME using the second process solution or third process solution, or to perform a fourth electroetching stage, such as a touch ECME, that uses the process solution that is used for the third stage or a fourth process solution such as an electroetching solution.

20

Alternately the modules A, B, C and D may be ECD and ECMD modules carrying out the first and second stages of the process using two different solutions as explained before. The number of each module will depend on the throughput of the first and the second stage processes. A robot would be used to transfer wafers between the various modules.

25

[00064] Figure 16 exemplifies a preferred system 200 using the single process module approach as applied to a two-step process. As shown in Figure 16, the system 200 comprising a first process module (PM1) 202 and a first process solution module (PSM1) 204. PM1 includes a process container 206 to hold process solutions and an electrode (anode) 208. The process container may have a volume less than two liters, preferably less than one liter. An upper

30

35

opening 210 of the process container is enclosed with a WSID 212. Above the WSID 212, a wafer 214 to be processed by the process of the present invention is held by a wafer carrier 217. The PSM1 comprises a process solution supply unit 216, a first valve 218, a second valve 220 and a drain 222. The supply unit 216 supplies fresh process solutions to the process container via 5 the first valve 218. The used solutions from the process container 206 is delivered back to the supply unit or to the drain 222 via the second valve 220.

[00065] Referring to Figure 16, the process supply unit 216 comprises a first tank 224 to store the first solution for the first stage of the process, a second tank 226 to store the second solution for the second stage of the process. Descriptions of the first solution, second solution, 10 first stage and second stage are given in the above description. When the used solutions are received by the unit 216, their additive and plating solution chemistries are checked and then replenished so that the tanks 224, 226 always keep process solutions with the right chemistries. The supply unit 216 also includes a rinse tank 228 to store DI water. DI water is used to clean 15 the process container 206 before the beginning of each process stage to. DI water may come directly from a DI line rather than from a tank. The tanks 224, 226 and 228 are connected to the valve 218 through supply lines 224', 226' and 228'. The valve 218 is connected to the process container 206 through a line 230. Further, used solutions (first, second and the rinsing solutions) are brought to the valve 220 through the line 232. From the valve 220, the first solution is taken 20 to first tank via line 234, the second solution is taken to second tank via line 236. The rinsing solution from the valve 220 is directed to the drain 222.

[00066] In an exemplary process sequence, at the first stage of the process, the first process solution from the first solution tank 224 of the PSM1 is delivered, via the valve 218, to the process solution container 206 of the PM1 and circulated back through return line 236. After the wafer 214 is processed the valve 218 is turned to DI supply and DI water from the rinse tank 228 is delivered to the process container 206 via the valve 218 to clean the process container 25 from the residues of the first solution. During the cleaning, the valve 218 may be periodically turned off and the valve 220 is turned on to direct the used rinsing solution to the drain 222. After the rinsing the second stage of the process is performed similar to the first stage but using the fresh second solution from the second tank 226 and delivering the used second solution back 30 to second solution tank 226 for the replenishment and storage purposes. After the second stage of the process, the process container is once again rinsed for the following wafer to be processed with the process of the present invention. It should be noted that there are many ways of feeding the various solutions to the process module. The example given here is just one of many possibilities. In case the two solutions used in this example are compatible, the rinse steps in 35 between may be skipped and small amount of intermixing between the solutions may be allowed.

[00067] It should be understood, of course, that the foregoing relates to preferred embodiments of the invention and that modifications may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. An electrochemical processing method for operating upon a wafer, the wafer having a top surface with first and second cavities disposed thereon, the first cavity having a narrower width than a second cavity, and a conductive layer having a conductive top surface associated therewith disposed on the top surface of the wafer and on the first and second cavities, the method comprising:

performing electrochemical deposition on the conductive layer of the wafer using a first electrolyte solution having a first conductive material therein to result in at least the first cavity being at least partially filled with the first conductive material; and

performing electrochemical mechanical deposition on the conductive layer of the wafer in which the first cavity is at least partially filled with the first conductive material using a second electrolyte that has a second conductive material therein to result in at least some of any remaining cavity of the first and second cavities being further filled with the second conductive material, wherein physical contact and relative motion is maintained between the conductive top surface of the conductive layer disposed over the top surface of the wafer and a workpiece surface influencing device for at least a period of the electrochemical mechanical deposition.

2. A method according to claim 1 wherein the first electrolyte solution is different from the second electrolyte solution.

3. The method according to claim 2 wherein both the first electrolyte solution and the second electrolyte solution contain an accelerator additive and a suppressor additive.

4. The method according to claim 3 wherein acceleration activity within the second electrolyte solution is higher than the acceleration activity within the first electrolyte solution.

5. The method according to claim 2 wherein the steps of performing electrochemical deposition and performing electrochemical mechanical deposition are performed in different process modules and each of the first electrolyte solution and the second electrolyte solution are each delivered to a different one of the different process modules.

6. The method according to claim 2 wherein the first electrolyte solution is optimized to fill the first cavity without defects and wherein the second electrolyte solution is optimized for planar deposition.

7. The method according to claim 2 wherein the conductive layer is initially a seed layer and wherein the first electrolyte solution is selected based upon a characteristic of the seed layer.

8. The method according to claim 2 wherein the steps of performing electrochemical deposition and performing electrochemical mechanical deposition are performed in a same

process module and each of the first electrolyte solution and the second electrolyte solution are delivered to the same process module.

9. The method according to claim 8 further including the step of cleansing the same process module with a cleaning solution between the steps of performing electrochemical deposition and performing electrochemical mechanical deposition.

10. The method according to claim 1 wherein the first electrolyte solution is the same as the second electrolyte solution

11. The method according to claim 1 wherein the steps of performing electrochemical deposition and performing electrochemical mechanical deposition are performed in a same process module.

12. The method according to claim 11, wherein during at least a substantial period of the electrochemical deposition, deposition occurs without physical contact between the wafer and the workpiece surface influencing device

13. The method according to claim 12 wherein during the substantial period the electrochemical deposition occurs with the workpiece surface influencing device spaced a distance from the wafer, thereby allowing for the workpiece surface influencing device to operate as a shaping plate.

14. The method according to claim 11 wherein the step of performing electrochemical deposition occurs so that during substantially an entire period thereof the electrochemical deposition occurs without physical contact between the wafer and the workpiece surface influencing device.

15. The method according to claim 14 wherein the period of the electrochemical mechanical deposition is substantially an entire time that the step of performing electrochemical mechanical deposition is performed.

16. The method according to claim 1 wherein during substantially an entire period that the step of performing electrochemical mechanical deposition is performed the physical contact and the relative motion is maintained between the conductive top surface of the conductive layer disposed over the top surface of the wafer and the workpiece surface influencing device.

17. The method according to claim 16 wherein the step of performing electrochemical deposition occurs so that during substantially an entire period thereof the electrochemical deposition occurs without physical contact between the wafer and any workpiece surface influencing device.

18. The method according to claim 1 wherein the step of performing electrochemical deposition minimizes the formation of a conductive bump over the first cavity by applying a reverse pulse potential.

deposition occurs without physical contact between the wafer and any workpiece surface influencing device.

18. The method according to claim 1 wherein the step of performing electrochemical deposition minimizes the formation of a conductive bump over the first cavity by applying a reverse pulse potential.

19. The method according to claim 1 wherein the step of performing electrochemical mechanical deposition results in the conductive top surface of the conductive layer being planar and each of the first and second cavities being completely filled.

20. The method according to claim 1 wherein the step of performing electrochemical deposition is performed until a depth of the first cavity is less than the width of the first cavity.

21. The method according to claim 1 further including the step of performing electrochemical etching of the conductive layer after the step of performing electrochemical mechanical deposition.

22. The method according to claim 21 wherein during at least a period of the step of electrochemical etching the electrochemical etching occurs without physical contact between the wafer and a workpiece surface influencing device.

23. The method according to claim 21 wherein the step of performing electrochemical etching of the conductive layer uses electrochemical mechanical etching and during the step of performing electrochemical mechanical etching physical contact and relative motion is maintained between the conductive top surface of the conductive layer disposed over the top surface of the wafer and the workpiece surface influencing device for at least a period of the electrochemical mechanical etch.

24. The method according to claim 21 wherein the step of performing electrochemical etching uses an electrolyte solution that is also used during the steps of performing electrochemical deposition and performing electrochemical mechanical deposition.

25. The method according to claim 1 wherein, after the step of performing electrochemical mechanical deposition, repeating at least one of the steps of performing electrochemical deposition and performing electrochemical mechanical deposition until the any remaining cavity of the first and second cavities are completely filled with one of the first and second conductive materials.

26. The method according to claim 25 wherein the first and second conductive materials are the same.

30. The method according to claim 1 wherein the conductive material is copper.
31. An integrated circuit manufactured including the method of claim 1.

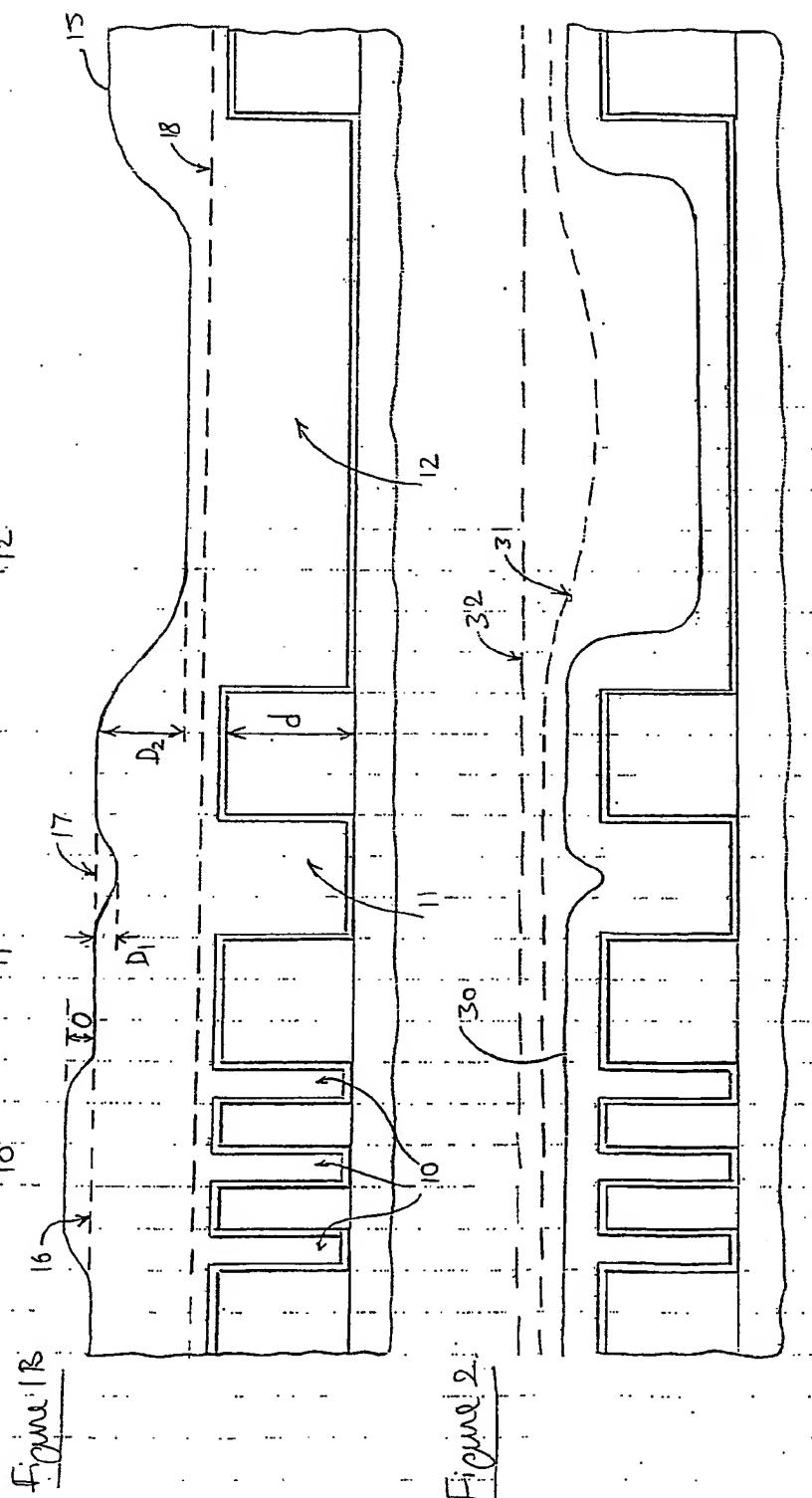
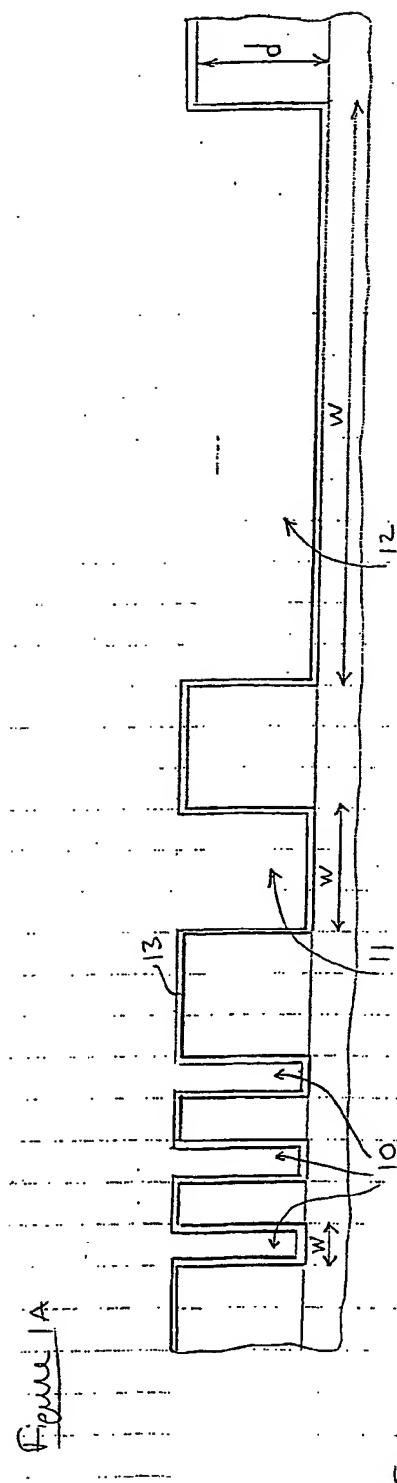


Figure 2

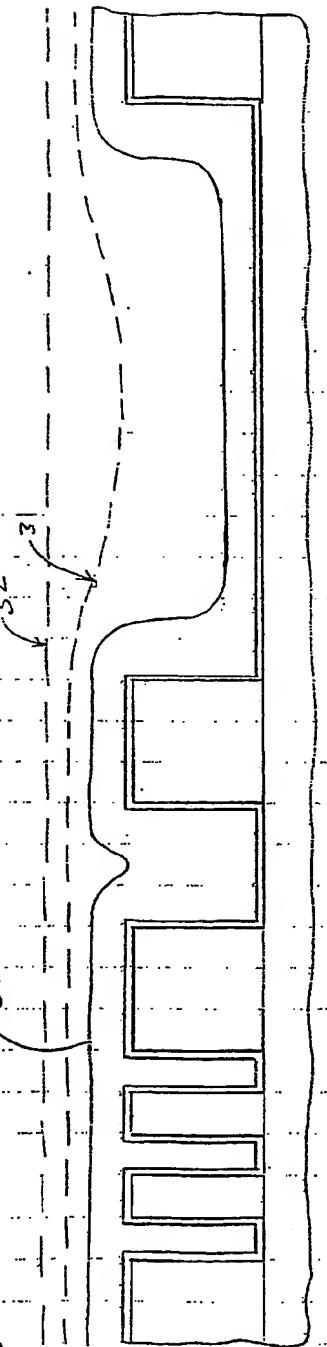


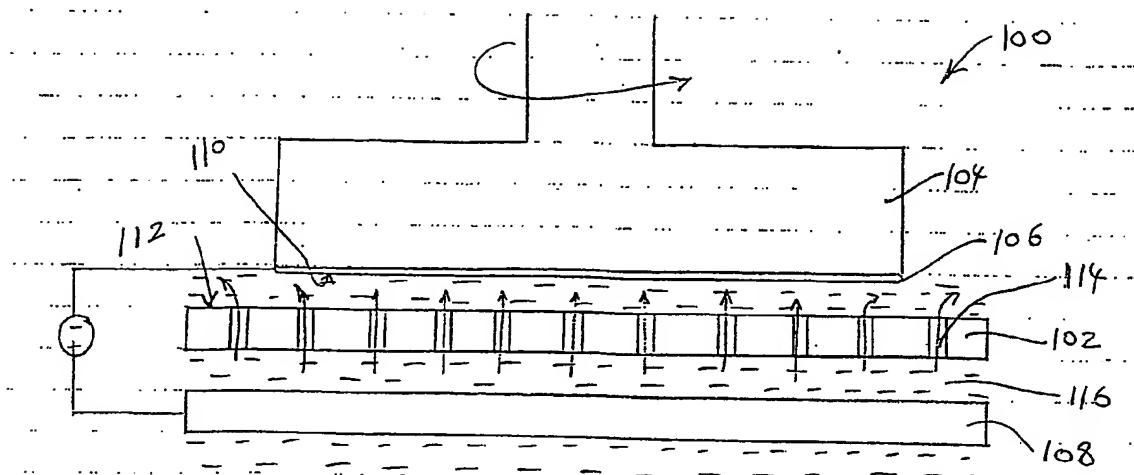
Figure 3

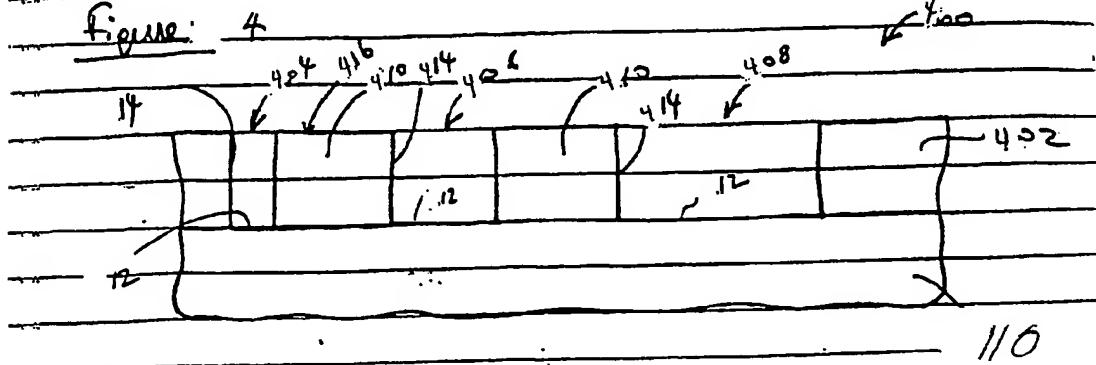
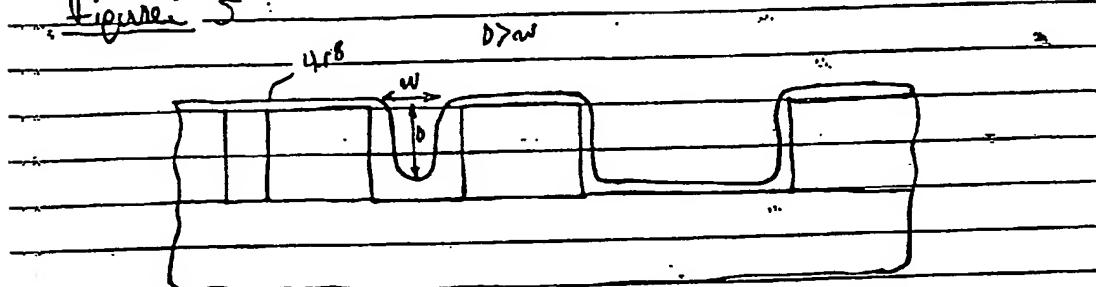
Figure 4Figure 5

Figure - 6A

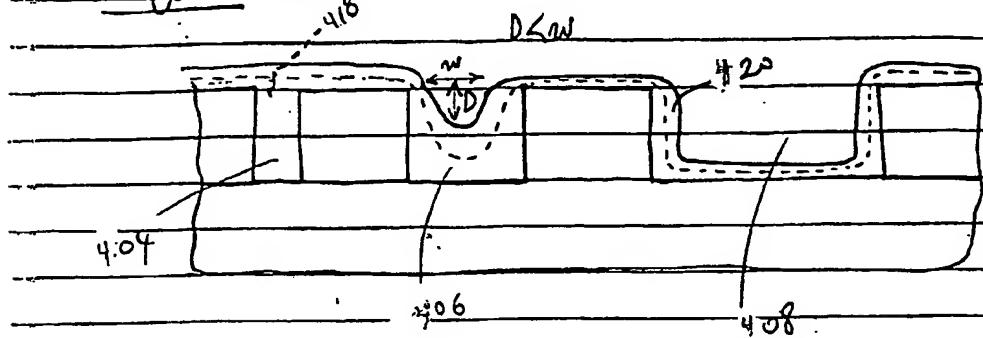
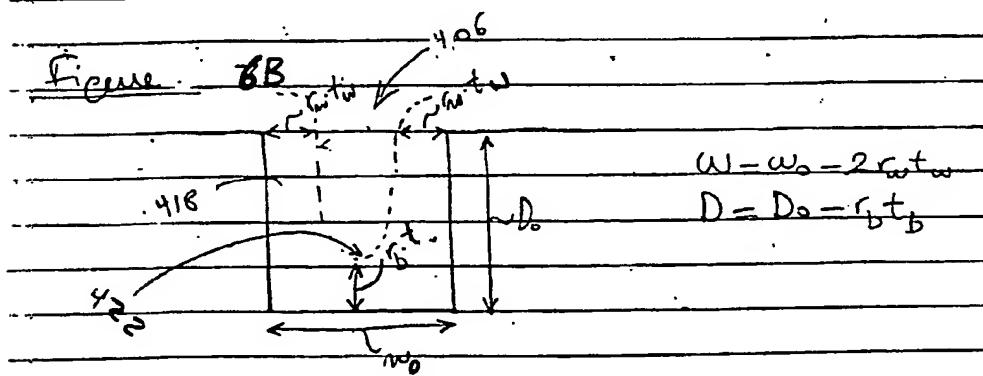


Figure 6B



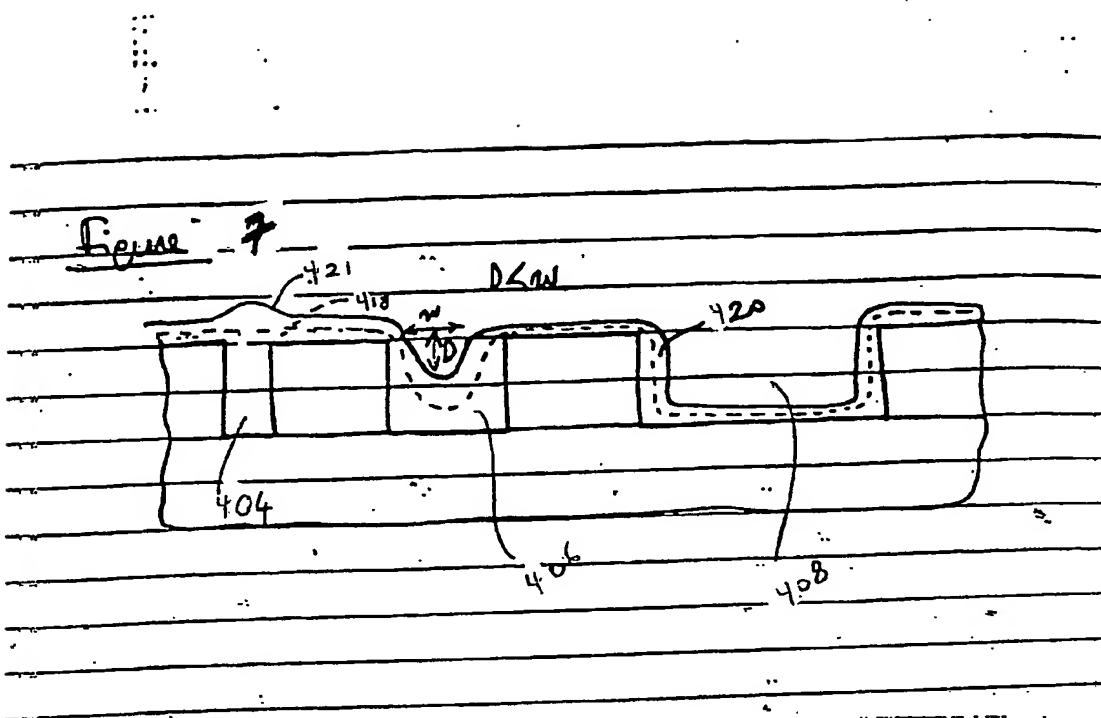


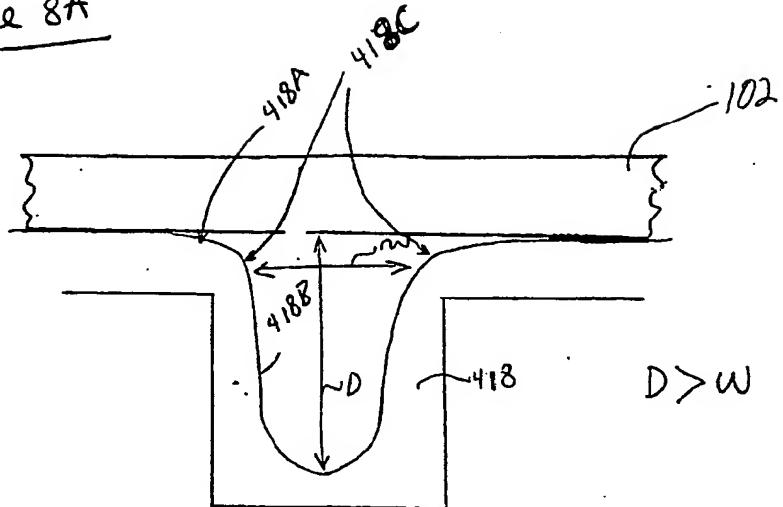
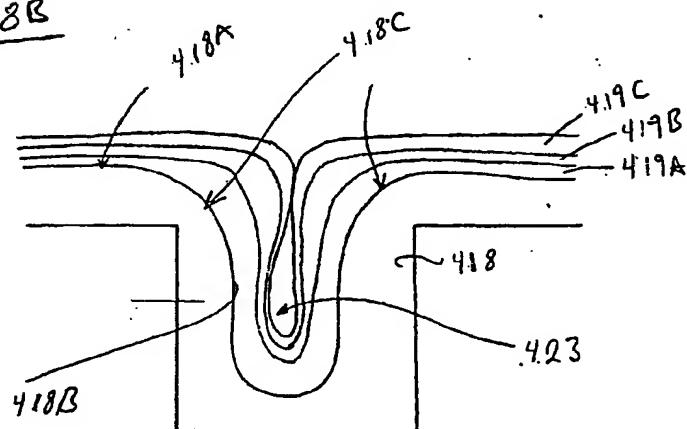
Figure 8AFigure 8B

Figure 9

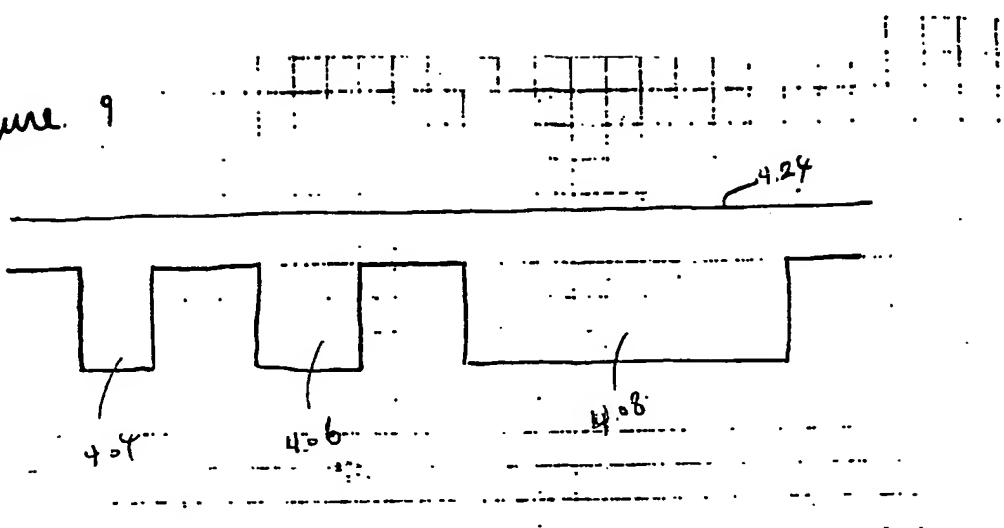


Figure 10

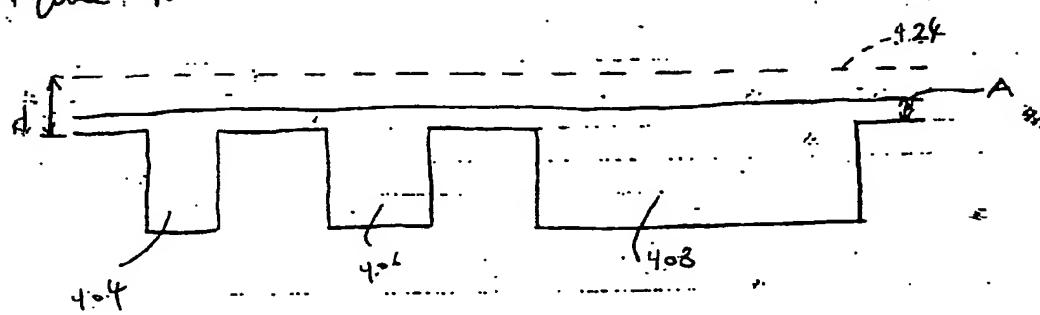


Figure 11

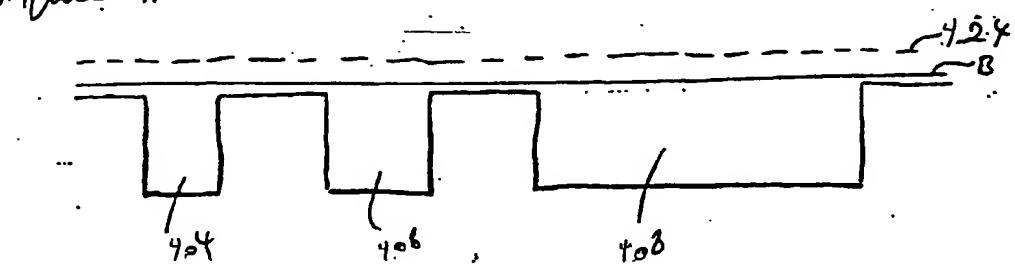
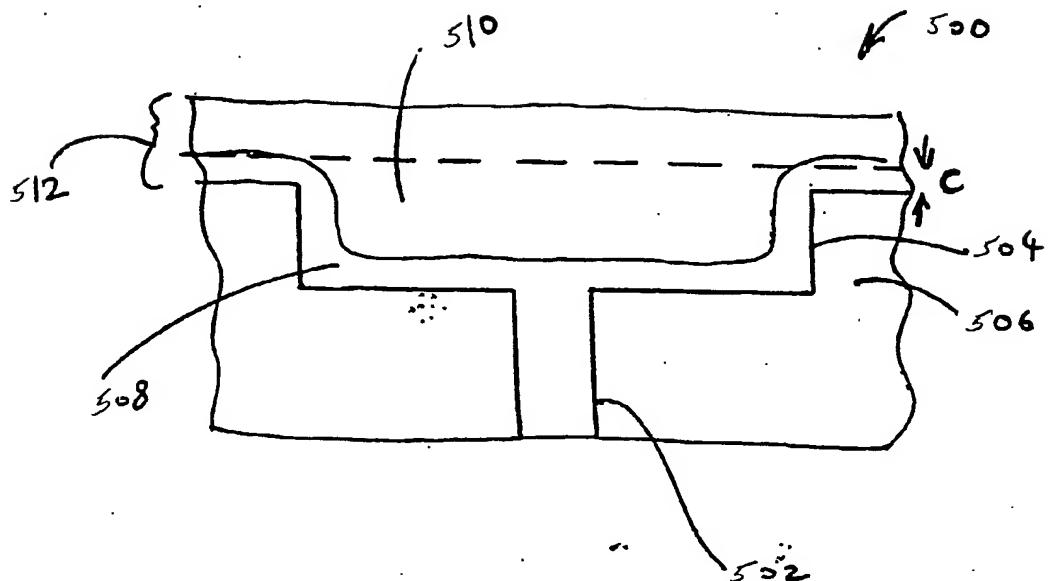
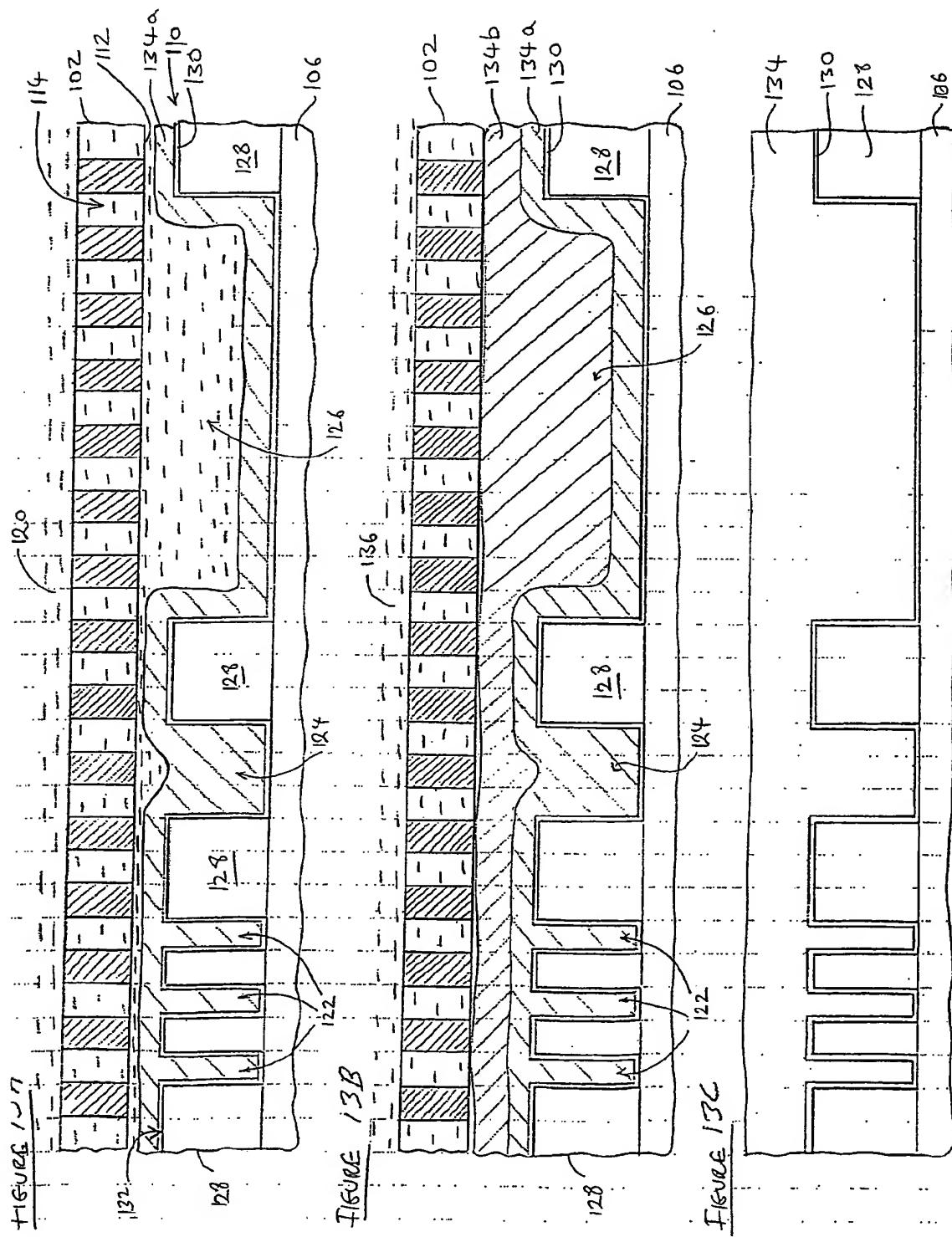


Figure 12



9 / 11



10 / 11

FIGURE 14A

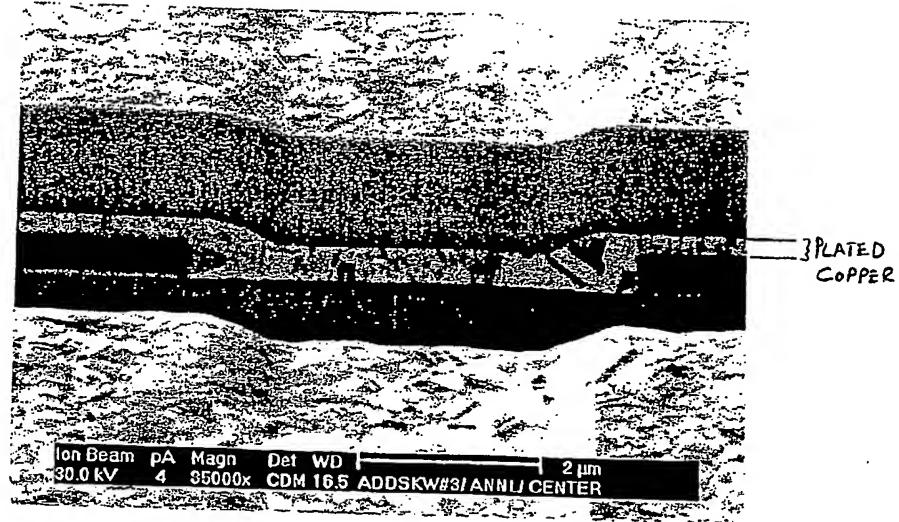
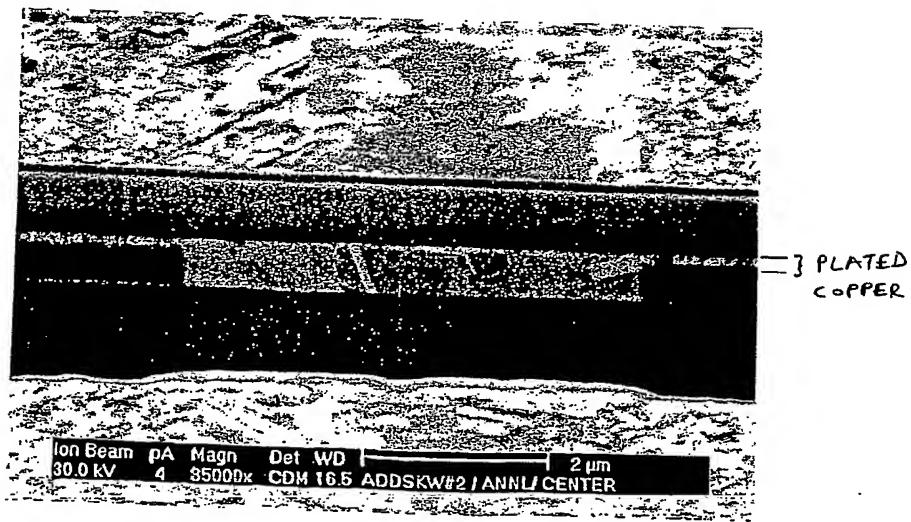


FIGURE 14B



11 / 11

FIGURE 16

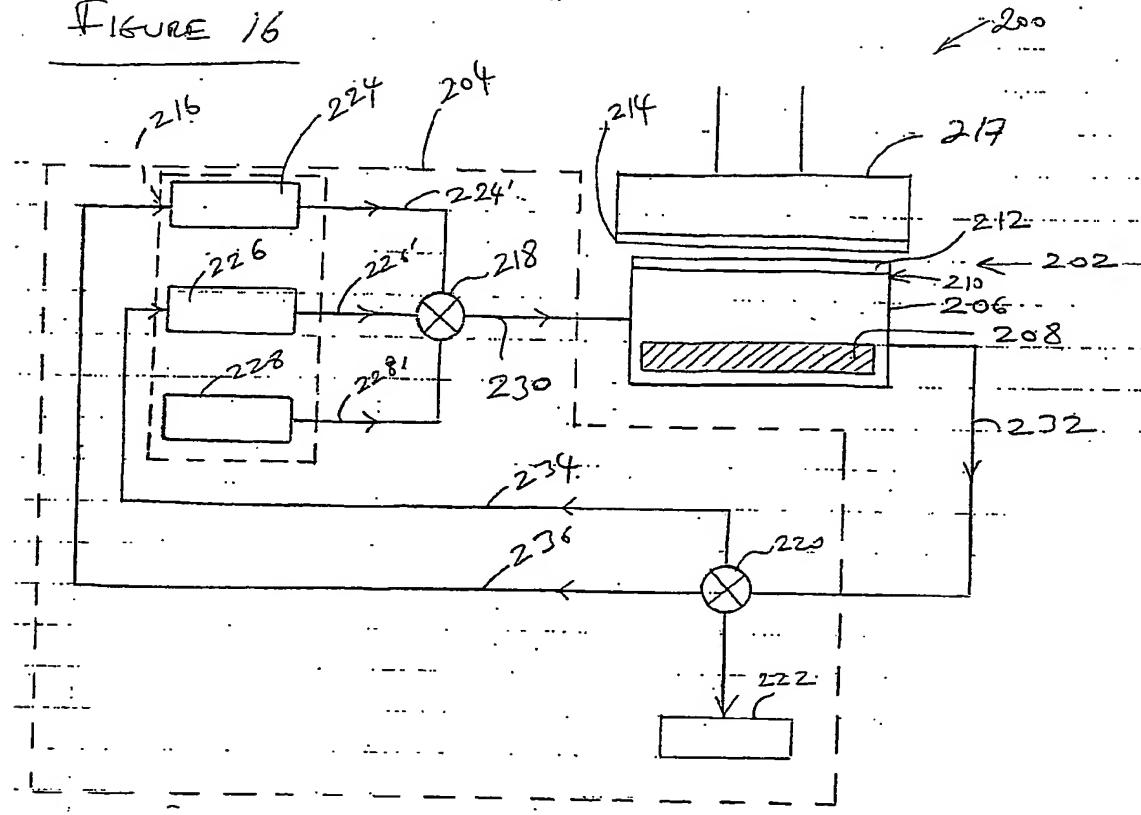
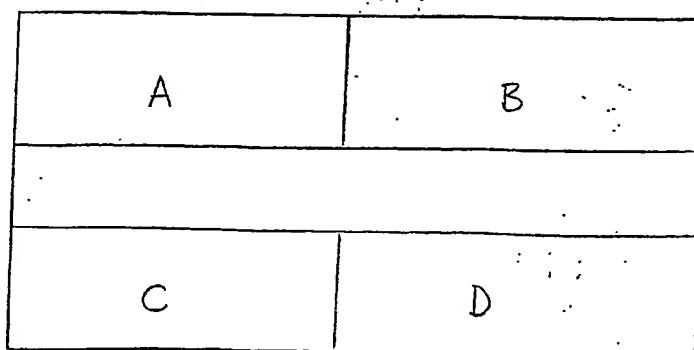


FIGURE 15



THIS PAGE BLANK (USPTO)

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- BLACK BORDERS**
- IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- FADED TEXT OR DRAWING**
- BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- SKEWED/SLANTED IMAGES**
- COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- GRAY SCALE DOCUMENTS**
- LINES OR MARKS ON ORIGINAL DOCUMENT**
- REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- OTHER: _____**

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.

THIS PAGE BLANK (USPC)